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TRANSMITTAL OF APPEAL BRIEF

Docket No.
BBNT-P01-128

In re Application of: Milliken et al.

Application No.	Filing Date	Examiner	Group Art Unit
09/938921	August 24, 2001	Q. N. Nguyen	2141

Invention: TERNARY CONTENT ADDRESSABLE MEMORY EMBEDDED IN A CENTRAL PROCESSING UNIT

TO THE COMMISSIONER OF PATENTS:

Transmitted herewith is the Appeal Brief in this application, with respect to the Notice of Appeal filed: April 6, 2006 .

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Dated: May 24, 2006

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Dated: 5/24/06 Signature: Joanne Ryan (Joanne Ryan)

Docket No.: BBNT-P01-128
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Milliken et al.

Application No.: 09/938921 Confirmation No.: 3501

Filed: August 24, 2001 Art Unit: 2141

For: TERNARY CONTENT ADDRESSABLE MEMORY EMBEDDED IN A CENTRAL PROCESSING UNIT Examiner: Q. N. Nguyen

APPEAL BRIEF

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This Appeal Brief is submitted in response to the non-final Office Action, dated February 6, 2006, and in support of the Notice of Appeal, filed April 6, 2006. The fees required under § 41.20(b)(2) are dealt with in the accompanying TRANSMITTAL OF APPEAL BRIEF.

I. REAL PARTY IN INTEREST

The real party in interest in this appeal is BBN Technologies Corp.

II. RELATED APPEALS, INTERFERENCES, AND JUDICIAL PROCEEDINGS

Appellant is unaware of any related appeals, interferences or judicial proceedings.

III. STATUS OF CLAIMS

Claims 1-16 and 18-21 are pending in this application.

Claims 1-16 and 18-21 were rejected in the Office Action, dated February 6, 2006, and are the subject of the present appeal. These claims are reproduced in the Claim Appendix of this Appeal Brief.

IV. STATUS OF AMENDMENTS

No amendments have been filed subsequent to the Office Action, dated February 6, 2006.

V. SUMMARY OF CLAIMED SUBJECT MATTER

In the paragraphs that follow, each of the independent claims and each dependent claim that is argued separately will be recited followed in parenthesis by examples of where support can be found in the specification and drawings.

Claim 1 recites a central processing unit (CPU) (100, Fig. 1) in a network device. The central processing unit includes an arithmetic logic unit (140, Fig. 1); and a ternary content addressable memory operatively coupled to the arithmetic logic unit within the CPU and configured to perform one or more matching operations (260, Fig. 2; Fig. 5; pg. 10, para. 0030; pg. 15, para. 0042).

Claim 2 recites that the one or more matching operations includes a network packet processing operation (pg. 15, para. 0043).

Claim 3 recites that the packet processing operation includes an address lookup operation (pg. 16, para. 0046).

Claim 4 recites that the address lookup operation includes an Internet Protocol (IP) address lookup operation (pg. 11, para. 0033).

Claim 5 recites that the one or more matching operations include a packet stuff/unstuff operation (pg. 15, para. 0043; pg. 16, para. 0046).

Claim 6 recites that the one or more matching operations includes a packet classification operation (pg. 16, para. 0046).

Claim 8 recites a first register configured to store a first 32-bit operand (310-380, Fig. 3; pg. 9, para. 0027; pg. 13, para. 0038); and a second register configured to store a second 32-bit operand (310-380, Fig. 3; pg. 9, para. 0027; pg. 13, para. 0038).

Claim 10 recites that the ternary content addressable memory includes a memory array including a group of 64-bit entries (pg. 11, para. 0032), and wherein, when performing the one or more matching operations, the ternary content addressable memory compares higher order bits of each entry of the memory array to the first 32-bit operand and compares lower order bits of each entry of the memory array to the second 32-bit operand (pg. 11, para. 0032).

Claim 16 recites a method for processing packets in a network device. The method includes receiving a packet (pg. 5, para. 0018; pg. 12, para. 0035; pg. 15, para. 0043); and processing the packet using a ternary content addressable memory resident within an arithmetic logic unit of the network device (pg. 15, paras. 0042 and 0043).

Claim 20 recites a system for forwarding packets in a network device. The system includes means for receiving at least one packet (130, Fig. 1; pg. 5, para. 0018; pg. 6, para. 0021; pg. 12, para. 0035; pg. 15, para. 0043); and means for processing the packet using a ternary content addressable memory (260, Fig. 2) resident within a central processing unit (100, Fig. 1) of the network device (260, Fig. 2; 100, Fig. 1; 130, Fig. 1; pg. 6, para. 0021; pg. 15, paras. 0042 and 0043).

Claim 21 recites an arithmetic logic unit (140) comprising a register unit (250, Fig. 2); an operations unit (270, Fig. 2); and a ternary content addressable memory coupled to the register unit and the operations unit within the arithmetic logic unit (260, Fig. 2; pg. 9, para. 0028; pg. 10, para. 0030; pg. 11, para. 0034).

VI. GROUND OF REJECTION TO BE REVIEWED ON APPEAL

A. Claims 1-6 stand rejected under 35 U.S.C. § 102(e) as anticipated by Kawana et al. (U.S. Patent No. 6,147,890).

B. Claims 1-6 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Kawana et al. (U.S. Patent No. 6,147,890).

C. Claims 7, 16, and 18-21 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Kawana et al. in view of Lineback ("Virage Announces First Embedded Content-Addressable Memory for Routers, Switches," www.siliconstrategies.com/article/showArticle.jhtml?articleID=10812751, June 19, 2000).

D. Claims 8-15 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Kawana et al. in view of Nataraj et al. (U.S. Patent No. 6,757,779).

VII. ARGUMENTS

A. The rejection of claims 1-6 under 35 U.S.C. § 102(e) as allegedly anticipated by Kawana et al. (U.S. Patent No. 6,147,890) should be reversed.

The initial burden of establishing a *prima facie* basis to deny patentability to a claimed invention always rests upon the Examiner. In re Oetiker, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). A proper rejection under 35 U.S.C. § 102 requires that a single reference teach every aspect of the claimed invention either explicitly or impliedly. Any feature not directly taught must be inherently present. Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 2 USPQ2d 1051 (Fed. Cir. 1987).

1. Claim 1.

Appellant's claim 1 is directed to a central processing unit (CPU) in a network device. The CPU includes an arithmetic logic unit and a ternary content addressable memory operatively coupled to the arithmetic logic unit within the CPU and configured to perform one or more matching operations. Kawana et al. does not disclose or suggest this combination of features.

For example, Kawana et al. does not disclose or suggest an arithmetic logic unit. The Examiner relies on field programmable gate array (FPGA) 140 in Fig. 1 of Kawana et al. as allegedly corresponding to an arithmetic logic unit (Office Action, pg. 2). Appellant submits that this element of Kawana et al. in no way corresponds to an arithmetic logic unit.

Fig. 1 of Kawana et al. depicts a CAM core-block 110 formed on one portion of an integrated circuit (IC) chip 102 and a group of programmable logic cells 130 that is part of a FPGA 140 (col. 7, lines 1-5). Kawana et al. in no way discloses or suggests that FPGA 140 corresponds to an arithmetic logic unit, as "arithmetic logic unit" is commonly known in the art. One skilled in the art would readily appreciate that an "arithmetic logic unit" is a specific kind of device (typically one with two inputs, a function select input, and one output containing the result of the function applied to the two inputs). A common example of an arithmetic logic unit is the old TTL 74181 arithmetic logic unit chip and its various descendants. One skilled in the art would readily appreciate that Kawana et al.'s FPGA 140 is not an arithmetic logic unit, as recited in claim 1. The Examiner has not pointed to any section of Kawana et al. that discloses that FPGA 140 is an arithmetic logic unit or explained why one skilled in the art would reasonably construe FPGA 140 to be an arithmetic logic unit. In fact, Appellant notes that Kawana et al. does not even disclose the terminology "arithmetic logic unit."

Kawana et al. does not further disclose or suggest a ternary content addressable memory (CAM) operatively coupled to the arithmetic logic unit within the CPU and configured to perform one or more matching operations, as also recited in claim 1. The Examiner relies on

element 110 in Fig. 1 of Kawana et al. as allegedly corresponding to the recited ternary CAM, element 100 as allegedly corresponding to the recited CPU, and points to col. 1, lines 33-42, and col. 6, lines 7-13, of Kawana et al. for support (Office Action, pp. 2-3). Appellant respectfully disagrees with the Examiner's interpretation of Kawana et al.

Element 110 in Fig. 1 of Kawana et al. corresponds to a CAM core-block. Kawana et al. in no way discloses or suggests that CAM core-block 110 corresponds to a ternary CAM, as recited in claim 1. Moreover, the Examiner does not explain why one skilled in the art at the time of Appellant's invention would have reasonably construed Kawana et al.'s CAM core-block 110 as a ternary CAM. Therefore, Kawana et al.'s CAM core-block 110 cannot reasonably be relied on as corresponding to a ternary CAM operatively coupled to an arithmetic logic unit within the CPU and configured to perform one or more matching operations, as recited in claim 1.

Even assuming, for the sake of argument, that one skilled in the art could reasonably construe CAM core-block 110 as a ternary CAM, Appellant submits that Kawana et al. does not disclose or suggest that element 100 corresponds to a CPU. Element 100 in Fig. 1 of Kawana et al. corresponds to an IC chip. Kawana et al. in no way discloses or suggests that IC chip 100 corresponds to a CPU, as recited in claim 1. Moreover, the Examiner does not explain why one skilled in the art at the time of Appellant's invention would have reasonably construed Kawana et al.'s IC chip 100 as a CPU.

Moreover, even assuming, for the sake of argument, that one skilled in the art could reasonably construe CAM core-block 110 as a ternary CAM and IC chip 100 as a CPU, Kawana et al. does not, as set forth above, disclose or suggest an arithmetic logic unit. Therefore, Kawana et al. cannot disclose CAM core-block 110 operatively coupled to an arithmetic logic

unit within a CPU and configured to perform one or more matching operations, as recited in claim 1. Instead, Kawana et al. specifically discloses CAM core-block 110 being connected to programmable logic cells 130 (see Fig. 1). Kawana et al. in no way discloses or suggests that programmable logic cells 130 correspond to an arithmetic logic unit.

At col. 1, lines 33-42, Kawana et al. discloses:

> Content Addressable Memory (CAM), is a special type of memory, typically RAM-based memory, with built in searching capabilities. As its name implies, in addition to being able to store and retrieve data items at addressable locations within the memory, CAM can also respond with the address of a memory location that has a data item that matches a user-specified search criterion. In effect, CAM memory cells behave like conventional RAM cells with embedded comparators capable of comparing a search key value against the contents of all memory cells of the CAM at once.

This section of Kawana et al. discloses that a CAM is a special type of memory with built in searching capabilities. This section of Kawana et al. in no way discloses or suggests a ternary CAM operatively coupled to an arithmetic logic unit within a CPU and configured to perform one or more matching operations, as recited in claim 1.

At col. 6, lines 7-13, Kawana et al. discloses:

> According to the invention, an optimized Content Addressable Memory "core" block is integrated onto a single Integrated Circuit (IC) chip along with a user-configurable logic such as a Field Programmable Gate Array (FPGA), with inputs and outputs to the CAM being provided as outputs and inputs, respectively, to programmable cells of the FPGA.

This section of Kawana et al. discloses the integration of a CAM onto a single IC chip along with a user-configurable FPGA. This section of Kawana et al. in no way discloses or suggests a ternary CAM operatively coupled to an arithmetic logic unit within a CPU and configured to perform one or more matching operations, as recited in claim 1.

For at least the foregoing reasons, Appellant submits that the rejection of claim 1 under 35 U.S.C. § 102(e) based on Kawana et al. is improper. Accordingly, Appellant requests that the rejection be reversed.

2. Claim 2.

Claim 2 depends from claim 1. Therefore, claim 2 is not anticipated by Kawana et al. for at least the reasons given above with respect to claim 1. Moreover, this claim recites an additional feature not disclosed or suggested by Kawana et al.

Claim 2 recites that the one or more matching operations include a network packet processing operation. The Examiner relies on col. 1, lines 51-55, of Kawana et al. for allegedly disclosing the above feature of claim 2 (Office Action, pg. 3). Appellant respectfully disagrees with the Examiner's interpretation of Kawana et al.

At col. 1, lines 51-55, Kawana et al. discloses:

> CAM-based memories are extremely valuable in database applications, high-speed network routing and bridging applications, data compression applications, memory caches, disk caches, and the like, since they completely automate the process of table searching.

This section of Kawana et al. discloses the use of CAM memories for a number of different applications, including high-speed network routing and bridging applications. This section of Kawana et al. does not disclose or suggest one or more matching operations that includes a network packet processing operation, as recited in claim 2. In fact, Kawana et al. does not even mention a "packet."

For at least these additional reasons, Appellant submits that the rejection of claim 2 under 35 U.S.C. § 102(e) based on Kawana et al. is improper. Accordingly, Appellant requests that the rejection be reversed.

3. Claim 3.

Claim 3 depends from claim 2. Therefore, claim 3 is not anticipated by Kawana et al. for at least the reasons given above with respect to claim 2. Moreover, this claim recites an additional feature not disclosed or suggested by Kawana et al.

Claim 3 recites that the packet processing operation includes an address lookup operation. The Examiner relies on col. 1, lines 51-55, of Kawana et al. for allegedly disclosing the above feature of claim 3 (Office Action, pg. 3). Appellant respectfully disagrees with the Examiner's interpretation of Kawana et al.

Col. 1, lines 51-55, of Kawana et al. is reproduced above. This section of Kawana et al. discloses the use of CAM memories for a number of different applications, including high-speed network routing and bridging applications. This section of Kawana et al. does not disclose a packet processing operation that includes an address lookup operation, as recited in claim 3. In fact, Kawana et al. does not even mention a "packet."

For at least these additional reasons, Appellant submits that the rejection of claim 3 under 35 U.S.C. § 102(e) based on Kawana et al. is improper. Accordingly, Appellant requests that the rejection be reversed.

4. Claim 4.

Claim 4 depends from claim 3. Therefore, claim 4 is not anticipated by Kawana et al. for at least the reasons given above with respect to claim 3. Moreover, this claim recites an additional feature not disclosed or suggested by Kawana et al.

Claim 4 recites that the address lookup operation includes an Internet Protocol (IP) address lookup operation. The Examiner relies on col. 1, lines 51-55, of Kawana et al. for allegedly disclosing the above feature of claim 4 (Office Action, pg. 3). Appellant respectfully disagrees with the Examiner's interpretation of Kawana et al.

Col. 1, lines 51-55, of Kawana et al. is reproduced above. This section of Kawana et al. discloses the use of CAM memories for a number of different applications, including high-speed network routing and bridging applications. This section of Kawana et al. does not disclose an address lookup operation that includes an IP address lookup operation, as recited in claim 4.

For at least these additional reasons, Appellant submits that the rejection of claim 4 under 35 U.S.C. § 102(e) based on Kawana et al. is improper. Accordingly, Appellant requests that the rejection be reversed.

5. Claim 5.

Claim 5 depends from claim 1. Therefore, claim 5 is not anticipated by Kawana et al. for at least the reasons given above with respect to claim 1. Moreover, this claim recites an additional feature not disclosed or suggested by Kawana et al.

Claim 5 recites that the one or more matching operations includes a packet stuff/unstuff operation. The Examiner relies on col. 1, lines 44-50, of Kawana et al. for allegedly disclosing the above feature of claim 5 (Office Action, pg. 3). Appellant respectfully disagrees with the Examiner's interpretation of Kawana et al.

At col. 1, lines 44-50, Kawana et al. discloses:

> Typically CAMs have a masking capability so that the comparisons can be restricted to only certain bits within each memory location, and so that selected memory locations or ranges of memory locations can be excluded from the search. Inputs to the CAM (i.e., address input/output, data input/output, search word, etc.) are typically routed via interconnection circuitry.

This section of Kawana et al. discloses that CAMs have a masking capability. This section of Kawana et al. in no way relates to one or more matching operations that includes a packet stuff/unstuff operation, as recited in claim 5. Appellant notes that one skilled in the art would recognize that a packet stuff/unstuff operation is a complex match and replace operation and not

simply a matching operation. Kawana et al. in no way discloses or suggests a packet stuff/unstuff operation.

For at least these additional reasons, Appellant submits that the rejection of claim 5 under 35 U.S.C. § 102(e) based on Kawana et al. is improper. Accordingly, Appellant requests that the rejection be reversed.

6. Claim 6.

Claim 6 depends from claim 1. Therefore, claim 6 is not anticipated by Kawana et al. for at least the reasons given above with respect to claim 1. Moreover, this claim recites an additional feature not disclosed or suggested by Kawana et al.

Claim 6 recites that the one or more matching operations includes a packet classification operation. The Examiner relies on col. 1, lines 33-42, of Kawana et al. for allegedly disclosing the above feature of claim 6 (Office Action, pg. 3). Appellant respectfully disagrees with the Examiner's interpretation of Kawana et al.

Col. 1, lines 33-42, of Kawana et al. is reproduced above. This section of Kawana et al. discloses that CAMs have built in searching capabilities. This section of Kawana et al. in no way relates to one or more matching operations that includes a packet classification operation, as recited in claim 6. In fact, Kawana et al. does not even mention a "packet."

For at least these additional reasons, Appellant submits that the rejection of claim 6 under 35 U.S.C. § 102(e) based on Kawana et al. is improper. Accordingly, Appellant requests that the rejection be reversed.

B. The rejection of claims 1-6 under 35 U.S.C. § 103(a) as allegedly unpatentable over Kawana et al. (U.S. Patent No. 6,147,890) should be reversed.

In rejecting a claim under 35 U.S.C. § 103, the Examiner must provide a factual basis to support the conclusion of obviousness. In re Warner, 379 F.2d 1011, 154 USPQ 173 (CCPA 1967). Based upon the objective evidence of record, the Examiner is required to make the factual inquiries mandated by Graham v. John Deere Co., 86 S.Ct. 684, 383 U.S. 1, 148 USPQ 459 (1966). The Examiner is also required to explain how and why one having ordinary skill in the art would have been realistically motivated to modify an applied reference and/or combine applied references to arrive at the claimed invention. Uniroyal, Inc. v. Rudkin-Wiley Corp., 837 F.2d 1044, 5 USPQ2d 1434 (Fed. Cir. 1988).

In establishing the requisite motivation, it has been consistently held that the requisite motivation to support the conclusion of obviousness is not an abstract concept, but must stem from the prior art as a whole to impel one having ordinary skill in the art to modify a reference or to combine references with a reasonable expectation of successfully achieving some particular realistic objective. See, for example, Interconnect Planning Corp. v. Feil, 227 USPQ 543 (Fed. Cir. 1985). Consistent legal precedent admonishes against the indiscriminate combination of prior art references. Carella v. Starlight Archery, 804 F.2d 135, 231 USPQ 644 (Fed. Cir. 1986); Ashland Oil, Inc. v. Delta Resins & Refractories, Inc., 776 F.2d 281, 227 USPQ 657 (Fed. Cir. 1985).

1. Claim 1.

At the outset, Appellant submits that the rejection of claim 1 is improper. The Examiner does not point out the feature or features that are not disclosed by Kawana et al. Moreover, the Examiner does not set forth why it would have been obvious to incorporate the missing feature or features into the Kawana et al. system. The Examiner has not established a *prima facie* case of obviousness with respect to claim 1 (or its dependents).

In the rejection of claim 1 under 35 U.S.C. § 103(a), the Examiner appears to allege that Kawana et al. discloses all of the features recited in claim 1 (see Office Action, pp. 2-3). For at least the reasons given above with respect to the 35 U.S.C. § 102(e) rejection of claim 1 based on Kawana et al., Appellant submits that Kawana et al. does not disclose or suggest the combination of features recited in claim 1.

For at least the foregoing reasons, Appellant submits that the rejection of claim 1 under 35 U.S.C. § 103(a) based on Kawana et al. is improper. Accordingly, Appellant requests that the rejection be reversed.

2. Claim 2.

Claim 2 depends from claim 1. Therefore, claim 2 is patentable over Kawana et al. for at least the reasons given above with respect to claim 1. Moreover, this claim recites an additional feature not disclosed or suggested by Kawana et al.

Claim 2 recites that the one or more matching operations include a network packet processing operation. The Examiner relies on col. 1, lines 51-55, of Kawana et al. for allegedly disclosing the above feature of claim 2 (Office Action, pg. 3). Appellant respectfully disagrees with the Examiner's interpretation of Kawana et al.

Col. 1, lines 51-55, of Kawana et al. is reproduced above. This section of Kawana et al. discloses the use of CAM memories for a number of different applications, including high-speed network routing and bridging applications. This section of Kawana et al. does not disclose or suggest one or more matching operations that includes a network packet processing operation, as recited in claim 2. In fact, Kawana et al. does not even mention a "packet."

For at least these additional reasons, Appellant submits that the rejection of claim 2 under 35 U.S.C. § 103(a) based on Kawana et al. is improper. Accordingly, Appellant requests that the rejection be reversed.

3. Claim 3.

Claim 3 depends from claim 2. Therefore, claim 3 is patentable over Kawana et al. for at least the reasons given above with respect to claim 2. Moreover, this claim recites an additional feature not disclosed or suggested by Kawana et al.

Claim 3 recites that the packet processing operation includes an address lookup operation. The Examiner relies on col. 1, lines 51-55, of Kawana et al. for allegedly disclosing the above feature of claim 3 (Office Action, pg. 3). Appellant respectfully disagrees with the Examiner's interpretation of Kawana et al.

Col. 1, lines 51-55, of Kawana et al. is reproduced above. This section of Kawana et al. discloses the use of CAM memories for a number of different applications, including high-speed network routing and bridging applications. This section of Kawana et al. does not disclose to a packet processing operation that includes an address lookup operation, as recited in claim 3. In fact, Kawana et al. does not even mention a "packet."

For at least these additional reasons, Appellant submits that the rejection of claim 3 under 35 U.S.C. § 103(a) based on Kawana et al. is improper. Accordingly, Appellant requests that the rejection be reversed.

4. Claim 4.

Claim 4 depends from claim 3. Therefore, claim 4 is patentable over Kawana et al. for at least the reasons given above with respect to claim 3. Moreover, this claim recites an additional feature not disclosed or suggested by Kawana et al.

Claim 4 recites that the address lookup operation includes an Internet Protocol (IP) address lookup operation. The Examiner relies on col. 1, lines 51-55, of Kawana et al. for

allegedly disclosing the above feature of claim 4 (Office Action, pg. 3). Appellant respectfully disagrees with the Examiner's interpretation of Kawana et al.

Col. 1, lines 51-55, of Kawana et al. is reproduced above. This section of Kawana et al. discloses the use of CAM memories for a number of different applications, including high-speed network routing and bridging applications. This section of Kawana et al. does not disclose an address lookup operation that includes an IP address lookup operation, as recited in claim 4.

For at least these additional reasons, Appellant submits that the rejection of claim 4 under 35 U.S.C. § 103(a) based on Kawana et al. is improper. Accordingly, Appellant requests that the rejection be reversed.

5. Claim 5.

Claim 5 depends from claim 1. Therefore, claim 5 is patentable over Kawana et al. for at least the reasons given above with respect to claim 1. Moreover, this claim recites an additional feature not disclosed or suggested by Kawana et al.

Claim 5 recites that the one or more matching operations includes a packet stuff/unstuff operation. The Examiner relies on col. 1, lines 44-50, of Kawana et al. for allegedly disclosing the above feature of claim 5 (Office Action, pg. 3). Appellant respectfully disagrees with the Examiner's interpretation of Kawana et al.

Col. 1, lines 44-50, of Kawana et al. is reproduced above. This section of Kawana et al. discloses that CAMs have a masking capability. This section of Kawana et al. in no way relates to one or more matching operations that includes a packet stuff/unstuff operation, as recited in claim 5. Appellant notes that one skilled in the art would recognize that a packet stuff/unstuff operation is a complex match and replace operation and not simply a matching operation. Kawana et al. in no way discloses or suggests a packet stuff/unstuff operation.

For at least these additional reasons, Appellant submits that the rejection of claim 5 under 35 U.S.C. § 103(a) based on Kawana et al. is improper. Accordingly, Appellant requests that the rejection be reversed.

6. Claim 6.

Claim 6 depends from claim 1. Therefore, claim 6 is patentable over Kawana et al. for at least the reasons given above with respect to claim 1. Moreover, this claim recites an additional feature not disclosed or suggested by Kawana et al.

Claim 6 recites that the one or more matching operations includes a packet classification operation. The Examiner relies on col. 1, lines 33-42, of Kawana et al. for allegedly disclosing the above feature of claim 6 (Office Action, pg. 3). Appellant respectfully disagrees with the Examiner's interpretation of Kawana et al.

Col. 1, lines 33-42, of Kawana et al. is reproduced above. This section of Kawana et al. discloses that CAMs have built in searching capabilities. This section of Kawana et al. in no way relates to one or more matching operations that includes a packet classification operation, as recited in claim 6. In fact, Kawana et al. does not even mention a "packet."

For at least these additional reasons, Appellant submits that the rejection of claim 6 under 35 U.S.C. § 103(a) based on Kawana et al. is improper. Accordingly, Appellant requests that the rejection be reversed.

C. The rejection of claims 7, 16, and 18-21 under 35 U.S.C. § 103(a) as allegedly unpatentable over Kawana et al. (U.S. Patent No. 6,147,890) in view of Lineback ("Virage Announces First Embedded Content-Addressable Memory for Routers, Switches," www.siliconstrategies.com/article/showArticle.jhtml?articleID=10812751, June 19, 2000) should be reversed.

1. Claim 7.

Claim 7 depends from claim 1. The disclosure of Lineback does not remedy the deficiencies in the disclosure of Kawana et al. set forth above with respect to claim 1. Therefore, Appellant submits that claim 7 is patentable over Kawana et al. and Lineback, whether taken alone or in any reasonable combination, for at least the reasons given above with respect to claim 1.

2. Claims 16, 18, and 19.

Claim 16 is directed to a method for processing packets in a network device. The method includes receiving a packet; and processing the packet using a ternary content addressable memory resident within an arithmetic logic unit of the network device. Kawana et al. and Lineback, whether taken alone or in any reasonable combination, do not disclose or suggest this combination of features.

For example, Kawana et al. and Lineback do not disclose or suggest processing a packet using a ternary content addressable memory resident within an arithmetic logic unit of a network device. The Examiner admits that Kawana et al. does not disclose this feature (Office Action, pg. 4). The Examiner alleges that "Lineback teaches on-chip content addressable memories were generated to support hardware-based search engine functions, which are tailored for networking application, such as routers and switches" and points to paragraphs 1-3 of Lineback for support (Office Action, pg. 4). Appellant submits that this allegation by the Examiner does not address the above feature of claim 16. That is, even if Lineback could reasonably be construed to disclose on-chip content addressable memories (a point that Appellant does not concede), Appellant submits that claim 16 does not merely recite an on-chip content addressable memory. Instead, claim 16 specifically recites processing a packet using a ternary content addressable memory resident within an arithmetic logic unit of a network device. The Examiner does not point to any section of Lineback that discloses this feature.

In paragraphs 1-3, Lineback discloses the use of an on-chip content addressable memory. Lineback in no way discloses or suggests that the content addressable memory is resident within an arithmetic logic unit, as recited in claim 16. Therefore, Lineback cannot reasonably be relied on for disclosing processing a packet using a ternary content addressable memory resident within an arithmetic logic unit of a network device, as recited in claim 16.

For at least the foregoing reasons, Appellant submits that the rejection of claim 16 under 35 U.S.C. § 103(a) based on Kawana et al. and Lineback is improper. Accordingly, Appellant requests that the rejection be reversed.

Claims 18 and 19 depend from claim 16. Therefore, Appellant requests that the rejection of these claims be reversed for at least the reasons given above with respect to claim 16.

3. Claim 20.

Claim 20 is directed to a system for forwarding packets in a network device. The system includes means for receiving at least one packet and means for processing the packet using a ternary content addressable memory resident within a central processing unit of the network device. Kawana et al. and Lineback, whether taken alone or in any reasonable combination, do not disclose or suggest this combination of features.

For example, Kawana et al. and Lineback do not disclose or suggest means for processing a packet using a ternary content addressable memory resident within a central processing unit of the network device. The Examiner does not specifically address the features of claim 20. Instead, the Examiner references the rejection of claims 1, 3, 6, and 7 (Office Action, pg. 5). Claims 1, 3, 6, and 7, however, do not recite means for processing a packet using a ternary content addressable memory resident within a central processing unit of a network device, as recited in claim 20. Accordingly, a *prima facie* case of obviousness has not been established with respect to claim 20.

Nonetheless, as set forth above with respect to the rejection of claim 1 under 35 U.S.C. § 102(e) based on Kawana et al., Kawana et al. does not disclose a ternary content addressable memory resident within a central processing unit. Therefore, Kawana et al. cannot disclose or suggest means for processing a packet using a ternary content addressable memory resident within a central processing unit of a network device, as recited in claim 20.

Similarly, Lineback does not disclose or suggest a ternary content addressable memory resident within a central processing unit. Instead, Lineback merely discloses a content addressable memory being placed on-chip. Placing a content addressable memory "on-chip" is not the same as a ternary content addressable memory that is resident within a central processing unit. Therefore, Lineback cannot disclose or suggest means for processing a packet using a ternary content addressable memory resident within a central processing unit of a network device, as recited in claim 20.

Even assuming, for the sake of argument, that Lineback can reasonably be construed to disclose means for processing a packet using a ternary content addressable memory resident within a central processing unit of a network device (a point that Appellant does not concede), Appellant submits that one skilled in the art would not have been motivated to incorporate this alleged teaching of Lineback into the Kawana et al. system, absent impermissible hindsight. The Examiner does not explain why one skilled in the art would have been motivated to incorporate Lineback's alleged teaching of means for processing a packet using a ternary content addressable memory resident within a central processing unit of a network device into the Kawana et al. system. Accordingly, a *prima facie* case of obviousness has not been established with respect to claim 20.

For at least the foregoing reasons, Appellant submits that the rejection of claim 20 under 35 U.S.C. § 103(a) based on Kawana et al. and Lineback is improper. Accordingly, Appellant requests that the rejection be reversed.

4. Claim 21.

Claim 21 is directed to an arithmetic logic unit. The arithmetic logic unit includes a register unit; an operations unit; and a ternary content addressable memory coupled to the register unit and the operations unit within the arithmetic logic unit. Kawana et al. and Lineback do not disclose or suggest this combination of features.

For example, Kawana et al. and Lineback does not disclose or suggest a ternary content addressable memory coupled to a register and an operations unit within an arithmetic logic unit. The Examiner admits that Kawana et al. does not disclose this feature (Office Action, pp. 4-5). The Examiner alleges that "Lineback teaches on-chip content addressable memories were generated to support hardware-based search engine functions, which are tailored for networking application, such as routers and switches" and points to paragraphs 1-3 of Lineback for support (Office Action, pg. 4). Appellant submits that this allegation by the Examiner does not address the above feature of claim 21. That is, even if Lineback could reasonably be construed to disclose on-chip content addressable memories (a point that Appellant does not concede), Appellant submits that claim 21 does not merely recite an on-chip content addressable memory. Instead, claim 21 specifically recites a ternary content addressable memory coupled to a register and an operations unit within an arithmetic logic unit. The Examiner does not point to any section of Lineback that discloses this feature.

In paragraphs 1-3, Lineback discloses the use of an on-chip content addressable memory. Lineback in no way discloses or suggests that the content addressable memory is resident within an arithmetic logic unit, as recited in claim 21. Therefore, Lineback cannot reasonably be relied

on for disclosing a ternary content addressable memory coupled to a register and an operations unit within an arithmetic logic unit, as recited in claim 21.

Even assuming, for the sake of argument, that Lineback can reasonably be construed to disclose a ternary content addressable memory coupled to a register and an operations unit within an arithmetic logic unit (a point that Appellant does not concede), Appellant submits that one skilled in the art would not have been motivated to incorporate this alleged teaching of Lineback into the Kawana et al. system, absent impermissible hindsight. The Examiner alleges that "it would have been obvious ... to provide support hardware-based search engine functions by quickly examining incoming packets of information and forward them to other systems in the network in a few nanoseconds" and points to paragraph 3 of Lineback for support (Office Action, pp. 4-5). Appellant submits that the Examiner's motivation is merely a conclusory statement regarding an alleged benefit of the combination. Such motivation does not satisfy the requirements of 35 U.S.C. § 103.

At paragraph 3, Lineback discloses:

> Embedded CAM blocks can be used by routers and switches to quickly examine incoming packets of information and forward them to other systems in the network in a few nanoseconds. Virage believes integrated CAM chips will enable hardware-based search engines to speed the routing of e-mail, set quality of services for different Internet users, and handle other functions that are often implemented in slow, software-based lookup tables.

This section of Lineback does not disclose or suggest a ternary content addressable memory within an arithmetic logic unit. Moreover, this section of Lineback in no way discloses or suggests why one skilled in the art would seek to incorporate Lineback's alleged teaching of a ternary content addressable memory coupled to a register and an operations unit within an arithmetic logic unit into the Kawana et al. system. Appellant submits that the Examiner's motivation is based on impermissible hindsight.

For at least the foregoing reasons, Appellant submits that the rejection of claim 21 under 35 U.S.C. § 103(a) based on Kawana et al. and Lineback is improper. Accordingly, Appellant requests that the rejection be reversed.

D. The rejection of claims 8-15 under 35 U.S.C. § 103(a) as allegedly unpatentable over Kawana et al. (U.S. Patent No. 6,147,890) in view of Nataraj et al. (U.S. Patent No. 6,757,779) should be reversed.

1. Claims 8 and 9.

Claim 8 depends from claim 1. The disclosure of Nataraj et al. does not remedy the deficiencies in the disclosure of Kawana et al. set forth above with respect to claim 1. Therefore, Appellant submits that claim 8 is patentable over Kawana et al. and Nataraj et al., whether taken alone or in any reasonable combination, for at least the reasons given above with respect to claim 1. Moreover, claim 8 recites additional features not disclosed or suggested by Kawana et al. and Nataraj et al.

Claim 8 recites a first register configured to store a first 32-bit operand and a second register configured to store a second 32-bit operand. The Examiner admits that Kawana et al. does not disclose these features (Office Action, pg. 5). The Examiner alleges that "Nataraj teaches CAM array 1601 can be configured for x32, x64, x128 or x256 operation, wherein when the CAM array 1601 is in a x32 configuration, selecting the lower 32 signal lines of the data bus to provide comparand data to comparand register segments to perform operations (i.e., performing matching operation based on at least one of the first or second 32-bit operands)" and relies on Fig. 21 and col. 37, line 46, to col. 38, line 24, of Nataraj et al. for support (Office Action, pg. 5). Appellant notes that this allegation by the Examiner does not address the specifically recited features of claim 8. That is, the Examiner does not allege that Nataraj et al. discloses a first register configured to store a first 32-bit operand and a second register

configured to store a second 32-bit operand, as recited in claim 8. Instead, the Examiner makes general allegations regarding the operation of CAM array 1601. These general allegations do not address the specific features recited in claim 8. Thus, a *prima facie* case of obviousness has not been established with respect to claim 8.

Nataraj et al.'s Fig. 21 depicts comparand register segments C1-C8 (col. 37, lines 50-52). Nataraj et al. discloses that comparand register segments C1-C8 store comparand segments (col. 37, lines 50-52). Contrary to the Examiner's allegation, Nataraj et al. in no way discloses or suggests that a first comparand register segment of comparand register segments C1-C8 stores a first 32-bit operand and a second comparand register segment of comparand register segments C1-C8 stores a second 32-bit operand, as recited in claim 8.

At col. 37, line 46, to col. 38, line 24, Nataraj et al. discloses:

> FIG. 21 illustrates an embodiment of a comparand load circuit which may be used in the exemplary CAM device described above in reference to FIGS. 16-19 (i.e., 64-bit wide data bus 1604, and a CAM array 1601 that includes Z=8 row segments (S1-S8) per row, each row segment having W=32 CAM cells). A comparand register 2103 includes eight comparand register segments, C1-C8, to store as many as eight corresponding comparand segments. Comparand register segments C1, C3, C5 and C7 are coupled to receive comparand data from the lower 32 signal lines of the data bus 1604 (i.e., signal path 2106), while comparand register segments C2, C4, C6 and C8 are coupled to receive comparand data from a multiplexer circuit 2105 via signal path 2108. When the CAM array 1601 is in a x32 configuration, the multiplexer circuit 2105 selects the lower 32 signal lines of the data bus to provide comparand data to comparand register segments C2, C4, C6 and C8, such that all eight comparand register segments are coupled to receive the same 32-bit value from the data bus 1604. When the CAM array 1601 is configured for x64, x128 or x256 operation, the multiplexer circuit 2105 selects the upper 32 signal lines of the data bus to provide comparand data to comparand register segments C2, C4, C6 and C8, such that comparand register segment pairs C1/C2, C3/C4, C5/C6 and C7/C8 are coupled to receive a 64-bit data value from the data bus 1604. In the embodiment of FIG. 21, the multiplexer circuit is controlled by the configuration signal, SZ32 (a component of the CFG signal) to select either the lower or upper half of the data bus 1604 to source data for the even numbered comparand register segments.
>
> Comparand enable signals, CEN[8:1], are generated in accordance with the configuration signals (i.e., SZ32, SZ64, SZ128 and SZ256) and comparand

> segment select signals CSSEL1 and CSSEL0 to enable selected comparand register segments to be loaded with comparand data. More specifically, the configuration signals indicate the size of an incoming comparand word (i.e., x32, x64, x128 or x256) and, when the incoming comparand word is larger than the data bus (i.e., a x128 long comparand word or x256 long comparand word), the CSSEL1 and CSSEL0 signals are used to load a 64-bit component of the long comparand word into the appropriate pair of comparand register segments. In one embodiment, when the comparand word is a 64-bit value (i.e., SZ=64), the 64-bit comparand word is loaded into all four comparand register segment pairs simultaneously. Similarly, when the comparand word is a 32-bit value (i.e., SZ=32), the 32-bit comparand word is loaded into all eight comparand register segments simultaneously.

This section of Nataraj et al. discloses that a comparand register 2103 includes eight comparand register segments C1-C8. As set forth above, Nataraj et al. does not disclose or suggest that a first comparand register segment of comparand register segments C1-C8 stores a first 32-bit operand and a second comparand register segment of comparand register segments C1-C8 stores a second 32-bit operand, as recited in claim 8.

For at least these additional reasons, Appellant submits that the rejection of claim 8 under 35 U.S.C. § 103(a) based on Kawana et al. and Nataraj et al. is improper. Accordingly, Appellant requests that the rejection be reversed.

Since claim 9 depends from claim 8, Appellant requests that the rejection of claim 9 be reversed for at least the reasons given above with respect to claim 8.

2. Claim 10.

Claim 10 depends from claim 8. The disclosure of Nataraj et al. does not remedy the deficiencies in the disclosure of Kawana et al. set forth above with respect to claim 8. Therefore, Appellant submits that claim 10 is patentable over Kawana et al. and Nataraj et al., whether taken alone or in any reasonable combination, for at least the reasons given above with respect to claim 8. Moreover, claim 10 recites additional features not disclosed or suggested by Kawana et al. and Nataraj et al.

Claim 10 recites that the ternary content addressable memory includes a memory array including a group of 64-bit entries. Claim 10 also recites that, when performing the one or more matching operations, the ternary content addressable memory compares higher order bits of each entry of the memory array to the first 32-bit operand and compares lower order bits of each entry of the memory array to the second 32-bit operand. The Examiner appears to admit that Kawana et al. does not disclose these features (Office Action, pg. 6). The Examiner relies on col. 37, line 15 to col. 38, line 24, of Nataraj et al. for allegedly disclosing these features (Office Action, pg. 6). Appellant respectfully disagrees with the Examiner's interpretation of Nataraj et al.

At col. 37, line 15 to col. 38, line 24, Nataraj et al. discloses:

> In the ZY/2x2W mode (i.e., two row segments per group), the CSSEL signals cause select logic 2001 to enable the odd CEN signals CEN1, CEN3, etc. such that the same first portion of comparand data is written into the first comparand segments associated with the first row segments S1, S3, etc. of CAM array 1501. In a subsequent cycle, the CSSEL signals cause select logic 2001 to enable the even CEN signals CEN2, CEN4, etc. such that the same second portion of comparand data is written into the second comparand segments associated with the second row segments S2, S4, etc. The first and second portions of comparand data together form the entire (2W) comparand data. This methodology continues until, in the YxZW mode, the CEN signals are sequentially enabled to consecutively load each portion (W) of the ZW comparand data into one of the Z comparand segments. The operation of this embodiment is further illustrated by the example of FIG. 21.
>
> FIG. 21 illustrates an embodiment of a comparand load circuit which may be used in the exemplary CAM device described above in reference to FIGS. 16-19 (i.e., 64-bit wide data bus 1604, and a CAM array 1601 that includes Z=8 row segments (S1-S8) per row, each row segment having W=32 CAM cells). A comparand register 2103 includes eight comparand register segments, C1-C8, to store as many as eight corresponding comparand segments. Comparand register segments C1, C3, C5 and C7 are coupled to receive comparand data from the lower 32 signal lines of the data bus 1604 (i.e., signal path 2106), while comparand register segments C2, C4, C6 and C8 are coupled to receive comparand data from a multiplexer circuit 2105 via signal path 2108. When the CAM array 1601 is in a x32 configuration, the multiplexer circuit 2105 selects the lower 32 signal lines of the data bus to provide comparand data to comparand register segments C2, C4, C6 and C8, such that all eight comparand register segments are coupled to receive the same 32-bit value from the data bus 1604. When the CAM array 1601 is configured for x64, x128 or x256 operation, the

> multiplexer circuit 2105 selects the upper 32 signal lines of the data bus to provide comparand data to comparand register segments C2, C4, C6 and C8, such that comparand register segment pairs C1|C2, C3|C4, C5|C6 and C7|C8 are coupled to receive a 64-bit data value from the data bus 1604. In the embodiment of FIG. 21, the multiplexer circuit is controlled by the configuration signal, SZ32 (a component of the CFG signal) to select either the lower or upper half of the data bus 1604 to source data for the even numbered comparand register segments.
>
> Comparand enable signals, CEN[8:1], are generated in accordance with the configuration signals (i.e., SZ32, SZ64, SZ128 and SZ256) and comparand segment select signals CSSEL1 and CSSEL0 to enable selected comparand register segments to be loaded with comparand data. More specifically, the configuration signals indicate the size of an incoming comparand word (i.e., x32, x64, x128 or x256) and, when the incoming comparand word is larger than the data bus (i.e., a x128 long comparand word or x256 long comparand word), the CSSEL1 and CSSEL0 signals are used to load a 64-bit component of the long comparand word into the appropriate pair of comparand register segments. In one embodiment, when the comparand word is a 64-bit value (i.e., SZ=64), the 64-bit comparand word is loaded into all four comparand register segment pairs simultaneously. Similarly, when the comparand word is a 32-bit value (i.e., SZ=32), the 32-bit comparand word is loaded into all eight comparand register segments simultaneously.

This section of Nataraj et al. discloses the loading of comparand data into comparand register segments C1-C8. This section of Nataraj et al. in no way discloses or suggests that, when performing one or more matching operations, the ternary content addressable memory compares higher order bits of each entry of the memory array to the first 32-bit operand and compares lower order bits of each entry of the memory array to the second 32-bit operand, as recited in claim 10.

For at least these additional reasons, Appellant submits that the rejection of claim 10 under 35 U.S.C. § 103(a) based on Kawana et al. and Nataraj et al. is improper. Accordingly, Appellant requests that the rejection be reversed.

3. Claims 11-15.

Claims 11-15 depend directly or indirectly from claim 1. The disclosure of Nataraj et al. does not remedy the deficiencies in the disclosure of Kawana et al. set forth above with respect

to claim 1. Therefore, Appellant submits that claims 11-15 are patentable over Kawana et al. and Nataraj et al., whether taken alone or in any reasonable combination, for at least the reasons given above with respect to claim 1.

VIII. CONCLUSION

In view of the foregoing arguments, Appellant respectfully solicits the Honorable Board to reverse the Examiner's rejection of claims 1-16 and 18-21 under 35 U.S.C. §§ 102 and 103. Appellant believes no fee is due with this response other than as reflected on the enclosed Transmittal of Appeal Brief. However, if a fee is due, please charge our Deposit Account No. 18-1945, under Order No. BBNT-P01-128 from which the undersigned is authorized to draw.

Dated: May 24, 2006

Respectfully submitted,

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IX. CLAIM APPENDIX

1. In a network device, a central processing unit (CPU) comprising:

an arithmetic logic unit; and

a ternary content addressable memory operatively coupled to the arithmetic logic unit within the CPU and configured to perform one or more matching operations.

2. The CPU of claim 1 wherein the one or more matching operations includes a network packet processing operation.

3. The CPU of claim 2 wherein the packet processing operation includes an address lookup operation.

4. The CPU of claim 3 wherein the address lookup operation includes an Internet Protocol (IP) address lookup operation.

5. The CPU of claim 1 wherein the one or more matching operations includes a packet stuff/unstuff operation.

6. The CPU of claim 1 wherein the one or more matching operations includes a packet classification operation.

7. The CPU of claim 1 wherein the ternary content addressable memory is located within the arithmetic logic unit.

8. The CPU of claim 1 further comprising:

a first register configured to store a first 32-bit operand; and

a second register configured to store a second 32-bit operand.

9. The CPU of claim 8 wherein the ternary content addressable memory performs the one or more matching operations based on at least one of the first or second 32-bit operands.

10. The CPU of claim 8 wherein the ternary content addressable memory includes a memory array including a group of 64-bit entries, and

wherein, when performing the one or more matching operations, the ternary content addressable memory compares higher order bits of each entry of the memory array to the first 32-bit operand and compares lower order bits of each entry of the memory array to the second 32-bit operand.

11. The CPU of claim 1 wherein the ternary content addressable memory includes a memory array that includes a group of 64-bit entries.

12. The CPU of claim 11 wherein the memory array comprises 32 entries.

13. The CPU of claim 1 wherein, when performing the one or more matching operations, the ternary content addressable memory is configured to:

compare an operand to a group of entries.

14. The CPU of claim 13 wherein the ternary content addressable memory is further configured to:

set a first flag when the operand fails to match an entry in the group of entries, and

set a second flag when the operand matches multiple entries of the group of entries.

15. The CPU of claim 13 wherein, prior to comparing, the ternary content addressable memory is configured to:

sequentially load the group of entries from a succession of mask/value pairs transferred to the ternary content addressable memory.

16. A method for processing packets in a network device, comprising:

receiving a packet; and

processing the packet using a ternary content addressable memory resident within an arithmetic logic unit of the network device.

18. The method of claim 16 wherein the processing includes performing a matching operation using information in a header of the packet.

19. The method of claim 18 wherein the processing includes a packet classification operation.

20. A system for forwarding packets in a network device, comprising:

means for receiving at least one packet; and

means for processing the packet using a ternary content addressable memory resident within a central processing unit of the network device.

21. An arithmetic logic unit comprising:

a register unit;

an operations unit; and

a ternary content addressable memory coupled to the register unit and the operations unit within the arithmetic logic unit.

X. EVIDENCE APPENDIX

None.

XI. RELATED PROCEEDINGS APPENDIX

None.